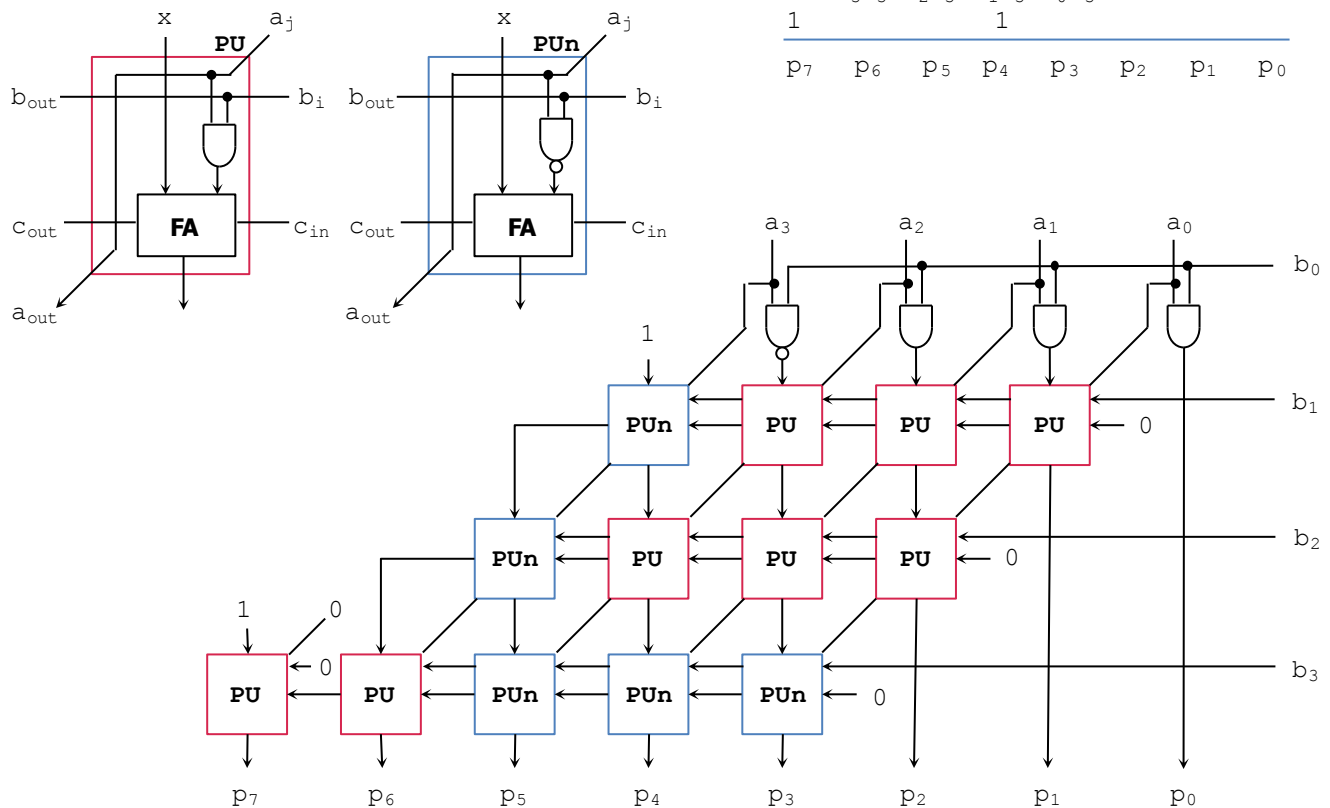


(Due date: **002/003**: Feb. 21st, **004**: Feb. 22nd, **006**: Feb. 23rd)

- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

- ✓ Refer to the [Tutorial: VHDL for FPGAs](#) for a list of examples.

- The figure depicts a 2's complement array multiplier for two 4-bit signed numbers. It is based on the basic unsigned multiplier with some adjustments.



- ✓ Create a new Vivado Project. Select the corresponding Artix-7 FPGA device (e.g.: the XC7A50T-1CSG324 FPGA device for the Nexys A7-50T).
- ✓ Write the VHDL code for this signed array multiplier. Synthesize your code.
 - Use the **Structural Description**: Create a separate .vhd file for the Full Adder, the Processing Unit (PU), the flipped Processing Unit (PUn) and the top file (Array Multiplier).
- ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use 'for loop'.
- ✓ Perform Functional Simulation and Timing Simulation of your design. **Demonstrate this to your TA.**
 - Your simulation might need more time than Vivado Simulator's default (1 us). For example, to add 5 us, you can go to the TCL console and type: `run 5 us`.
 - Note that you can represent your data as signed (2C) integers (use Radix → Signed Decimal).

- ✓ I/O Assignment: Generate the XDC file associated with your board.

- Suggestion:

Board pin names	SW7	SW6	SW5	SW4	SW3	SW2	SW1	SW0	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
Signal names in code	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀

- The board pin names are used by all the listed boards (Nexys A7-50T/A7-100T, Basys 3, Nexys 4/DDR). The I/Os listed here are all active high.

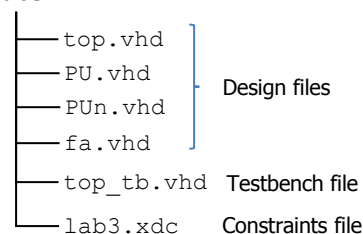
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA.**

- Submit (as a .zip file) the six generated files: VHDL code (4 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

- ✓ Your .zip file should only include one folder. Do not include subdirectories.

- It is strongly recommended that all your design files, testbench, and constraints file be located in a single directory. This will allow for a smooth experience with Vivado.

lab3



TA signature: _____

Date: _____